Conformance Test for Master Devices

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Abbreviations

addr.	Address
AT	Drive (amplifier) telegram
CP	Communication phase
DAT	Duration of AT
DMDT	Duration of MDT
DMST	Duration of MST
H	Hex
IDN	Ident number
IGS	Interests Group SERCOS-Interface e.V.
Mb/s	Mega baud per second
MDT	Master data telegram
MST	Master synchronization telegram
ppm	Parts per million

1 Introduction

As from April 2001, the Institute for Control Engineering of Machine Tools and Manufacturing Units (ISW) of the University of Stuttgart is authorized by the Interests Group SERCOS-Interface e.V. (IGS) to carry out Conformance Tests on SERCOS Devices according to the International Standard IEC/EN 61491. The aim of the Conformance Test is to ensure the compatibility and interoperability of SERCOS Devices from different vendors in multi-vendor environments. If a SERCOS Device passes the Conformance Test, a certificate can be applied for from the IGS. If any SERCOS-relevant changes are made to the Device's hardware or software, then the SERCOS Device must be retested. The Conformance Test Environment for SERCOS Master Devices (see Fig. 1) comprises of the Master Conformizer (a SERCOS Slave Emulator) running on a standard PC with an enhanced SERCOS interface card, an optical analyzer and a digital oscilloscope. For companies interested in performing their own tests, the Master Conformizer together with a passive PCI-SERCOS interface card can be ordered from the Interests Group SERCOS interface (IGS, Landhausstrasse 20, 70190 Stuttgart, Germany).

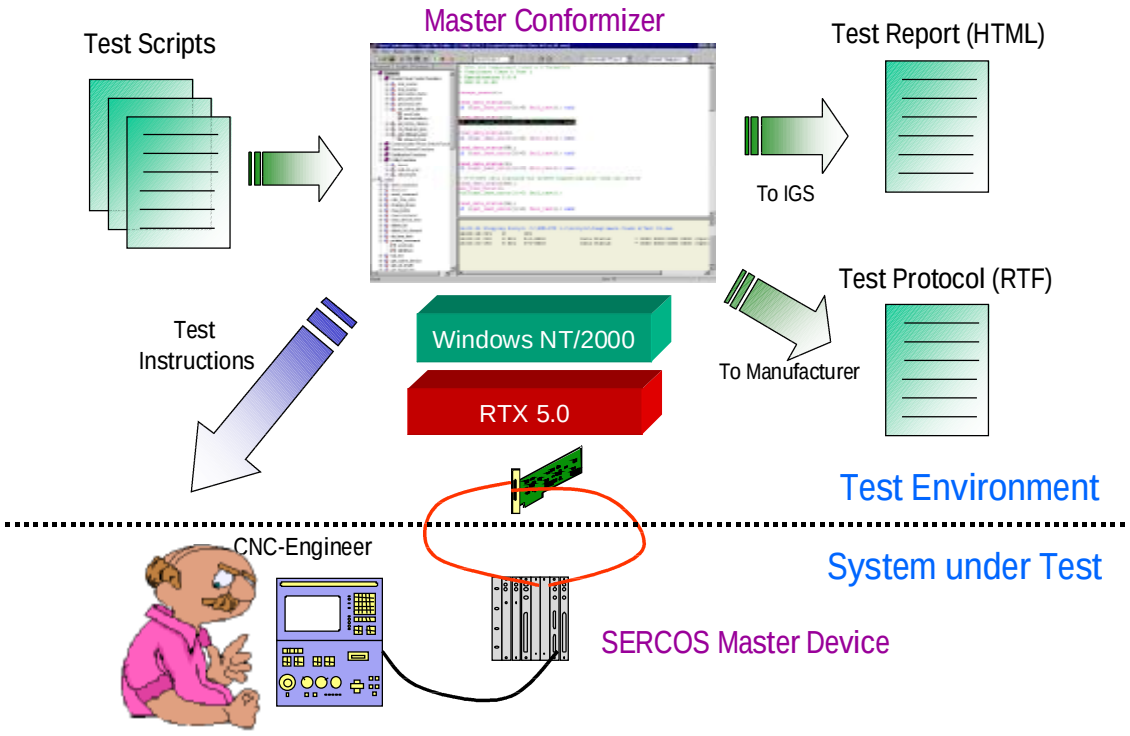

Fig. 1: Conformance Test Environment for Master Devices

The following sections in this document describe the test procedure, requirements and methods for SERCOS Master devices.

2 Test Procedure

Orders for Conformance Tests should be made in writing to the SERCOS interface Test Laboratory (ISW, University of Stuttgart, Seidenstrasse 36, 70174 Stuttgart, Germany). After an order has been placed, a date for the Conformance Test can be arranged. The duration of a Conformance Test for a SERCOS Master Device is typically two days, assuming that all requirements listed in Section 3 are met. On completion of the Conformance Test, a Test Report will be sent to the IGS. The customer will receive a copy of this report and a detailed Test Protocol of the test results. If the SERCOS Device passes the Conformance Test, a certificate confirming the conformance of this Device with the International Standard IEC/EN 61491 can be applied for in writing from the IGS (IGS, Landhausstrasse 20, 70190 Stuttgart, Germany). This certificate is only valid for devices with same catalog number. Any changes made to the hardware or software will invalidate this certificate and the device must be retested.

3 Test Requirements

In order to carry out the Conformance Test, the following requirements have to be met. A checklist listing all the information required for a Master Device Conformance Test is provided in Appendix A and should be completed and sent by the customer to the ISW at least 7 days before test begin. A qualified and experienced contact person must also be named who is capable of operating the Master Device. He/She is required to be present at ISW for the entire duration of the Conformance Test.

3.1 Master Device Requirements

The SERCOS Master Device to be tested, including all cable connections, manuals and documentation must arrive at ISW at least 7 days before the test begin. These requirements include:

- reference manuals for all the electrical and mechanical components (including a detailed description of the SERCOS-Interface),
- a power supply,
- all cable and connectors required for operation.

3.2 Asic Programming Requirements

The following information regarding the electrical components and asic programming of the Master Device must also be provided:

- asic type[1],
- frequency stability of the oscillator[2],
- receiver circuit,
- type of the optical receiver,
- programming of control bit POLRXD (control register address 1H.7) and REGMODE (addr. 1H.5)[3],
- programming of the SERCOS interface specific functions,
- programming of control bits RXDNRZ (addr. 1H.12) and PRESYNC (addr. 1H.8) [4].
- This information is used during the Conformance Test to check that the optical circuitry and asic setting have been correctly implemented.

3.3 Physical Test Requirements

In order to test the physical behavior of the Master Device, the Master device must allow the following optical test modes to be set:

- continuous light test,
- zero bit stream test,
- normal operation.

3.4 Logical Test Requirements

The following information is required in order to perform the logical tests:

- maximum number of Slave Devices that can be controlled in one ring[5],
- maximum supported baud rate[6] (2, 4, 8 or 16 Mbit/s),
- supported telegram types[7],
- supported operation modes[8],
- all operation mode bit combinations that are supported,
- start of communication cycle (software or signal CYCLE_CLK),

[1] SERCON 410B or SERCON 816.
[2] Must be less than 100 ppm.
[3] Their values depend on the receiver used.
[4] These registers must be set to certain values in order for the asic to operate correctly according to the SERCOS interface specification.
[5] All tests will be performed with one Slave Device and the maximum number of supported Slave Devices.
[6] All tests will be performed with the highest supported baud rate.
[7] Only the supported telegrams will be tested.
[8] Only the supported combinations will be tested.

- minimum supported communication cycle time[1],
- minimum cycle time and the granularity (see IEC 61491, annex D).

3.5 Required SERCOS-Interface Ident Numbers

In order for the Master Device to command a correct phase upshift for the Master Conformizer, the Master Device must be able to read from and write to a minimum set of System Parameters (see Tables 1 and 2). The logical tests can only be carried out if all of the following System Parameters are supported.

Ident Number	Name
S-0-0003	Shortest AT Transmission Starting Time (t_{1MIN})
S-0-0004	Transmit/Receive Transition Time (t_{ATMT})
S-0-0005	Minimum Feedback Processing Time (t_5)
S-0-0087	Transmit to Transmit Recovery Time (t_{ATAT}) (only if slave supports more than one drive)
S-0-0088[2]	Receive to Receive Recovery Time (t_{MTSY})
S-0-0096	Slave Arrangement
S-0-0185[3]	Length of Configurable Data Record in the AT
S-0-0186[3]	Length of Configurable Data Record in the MDT
S-0-0187[3]	List of Configurable Data in AT
S-0-0188[3]	List of Configurable Data in MDT

Table 1: Minimum Set of Ident Numbers to be Read

Ident Number	Name
S-0-0001	NC-Cycle Time (t_{Ncyc})
S-0-0002	Communication Cycle Time (t_{Scyc})

[1] All logical tests performed using one slave device will use the minimum supported communication cycle time down. If a cycle time less than 500 µs is supported than 500 µs will be used.
[2] Only required if slave supports more than one drive
[3] Only required if IDN S-0-0015 supports Telegram Type 7

S-0-0006	AT Transmission Starting Time (t_1)
S-0-0007	Feedback Acquisition Capture Time (t_4)
S-0-0008	Command Value Valid (t_3)
S-0-0009	Position of Data Record in MDT
S-0-0010	Length of MDT
S-0-0015	Telegram Type Parameter
S-0-0016[1]	Configuration List of AT
S-0-0024[1]	Configuration List of MDT
S-0-0032	Primary Operation Mode
S-0-0089	MDT Transmission Starting time (t_2)

Table 2: Minimum Set of Ident Numbers to be Written

[1] Only required if IDN S-0-0015 supports Telegram Type 7.

4 Test Methods

The conformance test includes a physical and a logical part.

4.1 Physical Part

4.1.1 Transmission Power

The optical transmission power is measured using the optical test mode continuous light. The transmission power must be within the specified limits (see IEC/EN 61491, 5.3.1).

4.1.2 Optical Curve Shape

The zero bit stream is measured at high and low attenuation. The curve shape must be within the specified optical signal envelope for the zero bit stream (see IEC/EN 61491, 5.4.1/5.4.2).

4.2 Logical Part

All tests are performed twice, once with Master Conformizer configured for one Slave Device and once with Master Conformizer configured for the maximum number of Slave Devices supported by the Master Device. If the Master Device supports more than 16 Slave Devices, then the Master Conformizer is configured for 16 Slave Devices.

4.2.1 Phase Switch

4.2.1.1 Behavior in CP_0

The Master Device must send MSTs with CP_0 and is not allowed to switch to CP1 until it has received 10 successive MSTs with CP_0.

4.2.1.2 Behavior in CP_1

The Master Device must:

a) Send telegrams using a communication cycle time equal to or greater than 1ms

b) And Send the MDT in a time window between 500µs and 700µs.

4.2.1.3 Behavior in CP_2

The Master Device must:

a) send MSTs with CP_2 phase information using a communication cycle time equal or greater than 1ms and

b) send MDTs in a time window between 500µs and 700µs.

c) be able to read and write data from all detected Slave Devices.

d) execute the procedure command CP_3 transition check (IDN S-0-0127) in order to initiate a phase upshift to CP_3.

e) wait for a command procedure acknowledgment before switching to CP_3 by sending MSTs with CP_3

f) and is not allowed to transmit any other service data between the procedure command acknowledgment and the end of the phase upshift.

4.2.1.4 Behavior in CP_3

The Master Device must:

a) send MSTs with CP_3 phase information using the selected communication cycle time T_{Scyc} (IDN S-0-0002) within the calculated jitter window J_{tScyc},

b) send the MDT at the MDT transmission starting time t_2 (IDN S-0-0089) within the calculated jitter window J_{t2}

c) execute the procedure command CP_4 transition check (IDN S-0-0128) to initiate a phase upshift to CP_4

d) wait for a command procedure acknowledgment before switching to CP_4 by sending MSTs with CP_4

e) and is not allowed to transmit any other service data between the procedure command acknowledgment and the end of the phase upshift.

4.2.1.5 Behavior in CP_4

The Master Device must:

a) send MSTs with CP_4 phase information using the selected communication cycle time T_{Scyc} (IDN S-0-0002) within the calculated jitter window

b) send the MDT at the MDT transmission starting time t_2 (IDN S-0-0089) within the calculated jitter window J_{t2}.

4.2.1.6 Phase Downshift

When performing a downshift from:

a) CP_4 to CP_0 the Master Device must send MSTs with CP_0 phase information using a communication cycle time equal or greater than 1ms.

b) CP_3 to CP_0 the Master Device must send MSTs with CP_0 phase information using a communication cycle time equal or greater than 1ms.

c) CP_2 to CP_0 the Master Device must send MSTs with CP_0 phase information using a communication cycle time equal or greater than 1ms.

d) CP_1 to CP_0 the Master Device must send MSTs with CP_0 phase information using a communication cycle time equal or greater than 1 ms.

4.2.2 Service Channel

All Service Channel tests are performed in CP_2, CP_3 and CP_4 with a Service Channel length of 2 bytes. A handshake timeout (a handshake taking longer than 10 Communication cycles) is not allowed to occur when testing the Service Channel.

4.2.2.1 Service Channel Handling

5 Ident numbers with 2-bytes and 4-bytes fixed length and variable length with 1-byte, 2-byte and 4-byte data strings must be read from and written to the Master Conformizer.

a) The ability of the Master Device to read and write all elements of a data block is to be checked.

b) The Master Device has to toggle the MHS-bit (bit 0) in the control word.

c) The Master Device must repeat the last step, if the Master Conformizer did not set the AHS-bit (bit 0) in the drive status word equal to the MHS-bit (bit 0) in the control word.

d) If the Master Conformizer sets the AHS-bit (bit 0) in the drive status equal to the value of the MHS-bit, but also sets the busy bit (bit 1) in the drive status word, the Master Device is not allowed to start a new transmission step until the busy bit is equal to 0 and the AHS-bit is equal to the MHS-bit.

e) No error is allowed to occur and the values read by the Master Device are compared with those of the Master Conformizer.

f) The Master Device reads and writes the data element of an Ident number, which has maximum and minimum input value elements, with a data value within the valid range of values. No error is allowed to occur and the values are compared with those of the Master Conformizer.

4.2.2.2 Error Detection

a) The Master Device writes to a write-protected element of an Ident number. The Master Device must register an error.

b) The Master Device reads and writes the data element of an Ident number, which has maximum and minimum elements, with a value above or below the range of valid values. The Master Device must register an error.

c) The Master Device should attempt to read and write the maximum and minimum elements of an Ident number, which does not support these elements. The Master Device must register an error.

4.2.3 Compliance Class A

The Master Device must be able to read from and write to all Ident numbers listed in Compliance Class A (see IEC/EN 61491, annex D) in CP_2, CP_3 and CP_4.

4.2.4 Time Slot Calculation

The Master Device must calculate the time slots according to the SERCOS interface specification IEC/EN 61491 (see chapter 6.3.1/2). The Master Conformizer provides default values for the times t_{1min}, t_{ATMT} and t_{MTSY} (see Table 3). This test is performed using one Slave device and with the maximum number of Slave Devices supported.

Ident Number	Name	Default Value
S-0-0003	Shortest AT transmission starting time (t_{1min})	20µs
S-0-0004	Transmit/receive transition time (t_{ATMT})	10µs
S-0-0005	Receive to receive recovery time (t_{MTSY})	10µs

Table 3: Default values for the Time Slot Calculation

a) The time slot calculation must fulfill the requirements for the shortest AT transmission starting time t_{1min} (IDN S-0-0003). Therefore the AT transmission starting time t_1 must fulfill the following conditions:

   i. for the first Slave Device: $t_{1.m} \geq t_{1min}$

   ii. for all other Slave Devices: $t_{1.m+1} \geq t_{1min} + DAT.m + 2 * J_{t1}$

b) The time difference between the last AT (AT.m) and the MDT must be equal to or greater than the transmit/receive transition time t_{ATMT} (IDN S-0-0004).

c) The MDT transmission starting time t_2 (S-0-0089) must therefore fulfill the following conditions for all Slave Devices:
   $t_2 \geq t_{1.m} + DAT.m + t_{ATMT}.m + J_{t1} + J_{t2}$

d) The time difference between the MDT and the next MST must be equal to or greater than the receive to receive recovery time t_{MTSY} (IDN S-0-0088).

e) The MDT transmission starting time t_2 must therefore fulfill the following conditions for all Slave Devices:
   $t_2 \leq t_{Scyc} – DMDT - DMST - t + t_{MTSYmax}.m + J_{t1} + J_{tScyc}$

4.2.5 Feedback Acquisition Capture Point & Command Value Valid Time

The Master Device must calculate the times feedback acquisition capture point t_4 (IDN S-0-0007) and command value valid time t_3 (IDN S-0-0008) according to the SERCOS-Interface specification (see IEC/EN 61491, chapter 6.3.1/2). The Master Conformizer provides default values for the necessary times t_5 and t_{MTSG} (see Table 4). This test is first performed with the Master Conformizer configured as a single Slave Device and afterwards configured for the maximum number of Slave Devices supported by the Master Device to be tested.

Ident Number	Name	Default Value
S-0-0005	Minimum feedback processing time (t_5)	80µs
S-0-0090	Command value proceeding time (t_{MTSG})	20µs

Table 4: Default values for calculation of t_3 and t_4

4.2.5.1 Command Value Valid Time t3 (IDN S-0-0008)

The Master Device must set the command value valid time t_3 to the same value for Slave Devices. The command value valid time t_3 must fulfill the following conditions for all Slave Devices:

$t_3 \leq t_{Scyc}$

$t_3 \leq t_2 + DMDT - J_{t2} - J_{tScyc}$

$t_3 \geq t_2 + DMDT + t_{MTSGmax} + J_{t2} + J_{tScyc}$

4.2.5.2 Feedback Acquisition Capture Point t_4 (IDN S-0-0007)

The Master Device must set the feedback acquisition capture point t_4 to the same value for all Slave Devices. The feedback acquisition capture point t_4 must fulfill the following conditions for all Slave Devices:

$t_4 \geq 0$

$t_4 \leq t_{Scyc} - t_{5max} - 2 * J_{tScyc}$

4.2.6 Error Handling

The Master Conformizer generates communication errors. The Master Device must react according to the SERCOS-Interface specification. All tests are performed in CP_2, CP_3 and CP_4.

4.2.6.1 Error Handling in CP_2

a) The Master Conformizer changes the drive address in the ATs to an address different from the selected drive address. The Master Device must recognize an AT failure if

during handshake timeout no response of the addressed drive is received. The Master Device must signal an error and return to CP0.

b) The transmission time of the AT is changed within a time window from 100µs to 300µs. No error is allowed to occur.

c) The transmission time of the AT is changed to a value below and above the time window 100µs to 300µs. The Master Device must recognize an AT failure if during handshake timeout no response of the addressed drive is received. The Master Device must signal an error and return to CP_0.

d) The Master Conformizer changes the length of the ATs. The Master Device must recognize an AT failure if during the handshake timeout no response from the addressed drive is received. The Master Device must signal an error and return to CP_0.

e) The Master Conformizer stops sending ATs. The Master Device must recognize an AT failure if during the handshake timeout no response from the addressed drive is received. The Master Device must signal an error and return to CP_0.

4.2.6.2 Error Handling in CP3

a) The Master Conformizer changes the drive address in two successive ATs to a address different from the selected drive address. The Master Device must recognize an AT failure, signal an error and return to CP_0.

b) The Master Conformizer sends ATs within the calculated jitter window J_{t1}. No error is allowed to occur.

c) The Master Conformizer sends ATs at a time below and above the calculated jitter window J_{t1}. The Master Device must recognize an AT failure, signal an error and return to CP_0.

d) The Master Conformizer sends two successive ATs at a time below and above the calculated jitter window J_{t1}. The Master Device must recognize an AT failure, signal an error and return to CP_0.

e) The Master Conformizer changes the length of two successive ATs. The Master Device must recognize an AT failure, signal an error and return to CP_0.

f) The Master Conformizer stops sending ATs. The Master Device must recognize an AT failure after two communication cycles, signal an error and return to CP_0.

4.2.6.3 Error Handling in CP_4

a) The Master Conformizer changes the drive address in two successive ATs to a address different from the selected drive address. The Master Device must recognize an AT failure, signal an error and return to CP_0.

b) The Master Conformizer sends ATs within the calculated jitter window J_{t1}. No error is allowed to occur.

c) The Master Conformizer sends ATs at a time below and above the calculated jitter window J_{t1}. The Master Device must recognize an AT failure, signal an error and return to CP_0.

d) The Master Conformizer sends two successive ATs at a time below and above the calculated jitter window J_{t1}. The Master Device must recognize an AT failure, signal an error and return to CP_0.

e) The Master Conformizer changes the length of two successive ATs. The Master Device must recognize an AT failure, signal an error and return to CP_0.

f) The Master Conformizer stops sending ATs. The Master Device must recognize an AT failure after two communication cycles, signal an error and return to CP_0.

5 References

IEC/EN 61491 : *Digital Interface for Communication between Controls and Drives for numerically controlled Machines*